Transmission of wireless neural signals through a 0.18m CMOS low-power amplifier

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Transmission of wireless neural signals through a 0.18µm CMOS low-power amplifier

Abstract— In the field of Brain Machine Interfaces (BMI) researchers still are not able to produce clinically viable solutions that meet the requirements of long-term operation without the use of wires or batteries. Another problem is neural compatibility with the electrode probes. One of the possible ways of approaching these problems is the use of semiconductor biocompatible materials (silicon carbide) combined with an integrated circuit designed to operate with low power consumption. This paper describes a low-power neural signal amplifier chip, named Cortex, fabricated using 0.18µm CMOS process technology with all electronics integrated in an area of 0.40mm². The chip has 4 channels, total power consumption of only 144µW, and is impedance matched to silicon carbide biocompatible electrodes.

I. INTRODUCTION

Although research with Brain Machine Interfaces (BMI) has evolved with great speed in recent years, researchers still do not have reliable BMI systems, which has prevented widespread clinical testing and, ultimately, assisting individuals with neurological and physical disabilities.

In order for BMI to effectively make use of the advances in robotic and computer technology, it is vital to find a biological interface that meets the requirements of long-term electrical reliability, low-power operation, and biocompatibility. These requirements are of special importance. First, commonplace systems are based on batteries that eventually discharge and must be replaced after short periods of time, resulting in additional maintenance requirements; Second, many systems rely on materials that may not have reliable biocompatibility, and can possibly erode with time, demanding costly and high-risk replacement procedures [1-2]. In this paper, our contribution focuses on addressing these two issues.

This project describes the development of a wireless BMI system – see Figure 1, with constraints of very low-power consumption and biocompatibility. Our solution relies on two features: (1) we use a chip designed to operate with a power consumption that is small enough for it to be powered by radio frequency antennas, dispensing with the need for batteries; (2) we use a probe manufactured from silicon carbide (SiC), a material that demonstrated excellent neural compatibility with murine mouse brain tissue in vivo [13].

This paper presents the first version of the Cortex chip, which is a 4-channel amplifier that magnifies neural signals to levels high enough for them to be processed by a computer.

Fig. 1. Conceptual diagram of the proposed BMI system, which integrates the Cortex chip, described in detail in this paper, with cubic silicon carbide electrodes (3C-SiC) and an RFID wireless interface.

II. CONCEPTS AND RELATED WORKS

A. Gliosis and Neural Implants

The introduction of neural interfaces inside the central nervous system (CNS) inevitably damages the delicate tissue which leads to the neural inflammatory response, gliosis [1-5]. Gliosis is a reactive cellular process concerning physiological changes in glial cells in an effort to restore the blood brain barrier and protect the CNS. However, if a device is recognized as a foreign object by the glia, it can lead to a chronic inflammatory reaction which normally results in the encapsulation of the device by tightly knit scar tissue, also named a glial scar. Glial scar encapsulation has been noted to lead to a reduction in reliability of the implanted devices, and is one of the leading causes preventing their therapeutic use. The search for alternative materials may help alleviate this issue and is currently an active research topic.

Fig. 2. A SiC optrode developed at USF [14]. The optrode features four platinum recording electrodes and an amorphous SiC coated SU-8 waveguide. The electrodes are designed to be connected to a neural signaling amplifier at the pads on the right side of the image.
B. Neural signal amplifiers

Many neural signal amplifiers have been developed since 2000 [8-11], but none of them meets our proposed needs. In former works, some authors implemented simple Operational Transconductance Amplifiers (OTA’s) for neural signal amplification based on older technologies (1500 nm to 500 nm). Modern designs are based on more advanced technologies, such as 0.18 µm CMOS, leading to lower power consumption and die area, which are mandatory characteristics for our project.

Many of the recent designs also have drawbacks. Some authors [11] completely avoid the use of on-chip (and even off-chip) capacitors, to minimize power consumption. This design decision forces them to use DC coupling (instead of AC coupling) at the amplifier input, forcing them to deal with DC component elimination a posteriori. This can be an issue because there might be a loss of data due to the circuitry. Other authors simply choose to use very large transistors [8] at the input to reduce flicker noise (which appears at very low frequencies), but this design increases the power consumption, even when using more advanced technologies.

III. THE CORTEX CHIP

A. Silicon Carbide (3C-SiC) Neural Interface

In a previous study [13], it was observed that cubic silicon carbide (3C-SiC) is highly compatible with CNS tissue in a murine mouse model. Therefore, in this work, we opted for 3C-SiC as the most adequate material to define a permanent implantable neuronal prosthesis. Figure 2 presents 6 µm thick, 7 mm long 3C-SiC optrode developed in our laboratory with four gold electrodes, an SU-8 optical waveguide, and amorphous SiC insulation. The tab contains 4 bonding pads to connect the electrodes to the proposed electronics.

B. Design of the Operational Transconductance Amplifier

An ideal implantable BMI not only includes material neural compatibility but it should also include the following: very low power consumption to operate without batteries, broadband data transmission, small area encapsulation (no off-chip components) and, avoid high power radio frequency operation, below the absorption limits of biological tissues. With these requirements in mind, we designed a special purpose Operational Transconductance Amplifier (OTA), detailed as follows.

Figure 3 shows the chain structure of our amplifier. It has two stages, each with 14.14 of voltage gain, and an output buffer for test purposes. The gain stages gm1 and gm2 are comprised of a fully differential OTA, featuring high open loop gain, low input referred noise, and high power supply rejection ratio (PSRR). Details of the OTA architecture are shown in Fig. 4. The gain per stage is defined by the ratio of the capacitances C2 and C1, leading, in this case, to a value of 23dB. Besides the gain, the capacitors act as high pass (C1) and low pass filters (C2 and C3). These filters are designed to reduce flicker and thermal noise inside the signal band.

Figures 3 and 4 present the architecture used in our Cortex amplifier and the schematic of the developed OTA respectively. Each amplifier stage has a gain of 14.14 V/V. The last stage of the Cortex architecture diagram shows two support buffers enabled only during test measurements with external equipment. It should be noted that the on-chip capacitors are very small (~4pF), which contributes to a significant reduction in power consumption.

Fig. 3. Regular two-stage OTA architecture with 14.14 V/V gain per stage (~200x total gain of ~46dB).

Fig. 4. Schematic of the Operational Transconductance Amplifier (OTA) and Common Mode Feed Back circuit (CMFB) used in each stage of the Cortex chip.

C. Wireless link

For the wireless functionality, we opted for an off-the-shelf solution. We chose the 915MHz PHY CM9011ff [12] from Chipus Microelectronics, illustrated in Figure 5; this choice was guided by the fact that its operation, in the range from ~1-3GHz, minimizes the channel loss for edge-to-edge coupling in biological strata.

In this solution, the data stream will be up to 800 kbps with 4 channels using a 10-bit 20kHz ADC; in accordance to the maximum specific absorption rate (1.6W/kg) defined by the Federal Communications Commission (FCC).

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Fig. 5. RFID PHY block diagram from the CM9011ff off-the-shelf chip developed by Chipus Microelectronics. It operates at 915MHz with 1.5µA for passive RFID tags.

IV. RESULTS

In this section, we present the results of functional tests for our integrated circuit. Figure 6a shows a photo of the die manufactured in 0.18um CMOS technology. The core dimensions without pads are X=572um and Y=782um.

The combined die was encapsulated in a QFN64 package, as presented in Figure 6b. Three of the packaged devices have been integrated with silicon carbide electrodes using the chip-on-board (COB) process. They will be implanted in rat brains for in-vivo tests in the next stage of development.

In Figure 7 we present the gain, in dB, of our system - while in Figure 8 we present the power supply rejection ratio (PSRR).

Fig. 7. Measured amplifier frequency response – showing a gain of 46dB (200x) up to 10kHz.

This signal was reproduced with two input amplitudes: 1mV and 100µV. The results of the amplification are shown in Figures 9 and 10. We are particularly interested in both the Local Field Potential (LFP / 5mV) and the Action Potential type (AP / 100µV) neural signals.

Fig. 8. Measured power supply rejection rate (PSRR) vs frequency – displaying a worst case value of 64dB.

We tested th IC with emulated neural signals (1mV and 100µV) which were loaded into a programmable signal generator and injected at the input of the Cortex chip.

Fig. 9. Measured Cortex amplified output data, using an input signal with 1mV amplitude (typical of LFP neural signals); green and yellow are the differential outputs from the Cortex chip; purple is from the oscilloscope math subtraction operation.
Fig. 10. Measured Cortex amplified output data, using an input signal with 100µV amplitude (typical of AP neural signals); green and yellow are the differential outputs from the Cortex chip; purple is from the oscilloscope math subtraction operation.

Tables I and II present the summary of the results obtained for the Cortex chip in comparison with previously published results for similar circuits. Table II shows that our chip has the following advantages: better PSRR and power consumption performance, smaller area per channel, and AC instead of DC coupling.

V. CONCLUSION

This paper presented the Cortex chip, a low-power neural signal amplifier fabricated in a 0.18µm CMOS process with all electronics integrated into an area of 0.40mm². The chip was designed with 4 channels and its total power consumption was only 144µW. It was designed to match the impedance of the SiC electrodes, thus enabling better neural compatibility of the entire system. Furthermore, it is integrated with a RFID PHY for wireless communication. The results showed that LFP/5mV and AP/100µV neural signals can be sampled by the system’s probe without distortion. Finally, the Cortex chip power consumption was remarkably low in accordance with the requisites of the project. Our design has demonstrated promising results as an integrated circuit for brain-machine interfacing, demonstrating its potential for in a future brain-controlled device.

TABLE I. SUMMARY OF SYSTEM PERFORMANCE

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<thead>
<tr>
<th>Feature</th>
<th>Other Authors</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regulated Supply Voltage</td>
<td>1.8V typ. (1.6V min. – 2.0V max.)</td>
<td></td>
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<tr>
<td>Regulator PSRR</td>
<td>80dB</td>
<td></td>
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<tr>
<td>Neural Signal Coupling</td>
<td>AC</td>
<td></td>
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<tr>
<td>Neural Signal Amplifier Gain</td>
<td>46dB (0.2 – 10kHz)</td>
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<tr>
<td>Input-Referred Noise</td>
<td>36µVrms (0.2 – 10kHz)</td>
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<tr>
<td>Number of Channels</td>
<td>4</td>
<td></td>
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<tr>
<td>Bandwidth</td>
<td>0.2kHz-10kHz</td>
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<tr>
<td>Process</td>
<td>Silterra, CMOS 0.18µm</td>
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TABLE II. IMPROVED FEATURES

<table>
<thead>
<tr>
<th>Feature</th>
<th>Other Authors</th>
<th>This Work</th>
</tr>
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<tbody>
<tr>
<td>Power (per channel)</td>
<td>80µW/Ch [8]</td>
<td>36µW/Ch</td>
</tr>
<tr>
<td>Regulator PSRR</td>
<td>5.5dB [9]</td>
<td>64dB</td>
</tr>
<tr>
<td>Chip Area (per channel)</td>
<td>0.160mm²/Ch [10]</td>
<td>0.111mm²/Ch</td>
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REFERENCES